WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell storing data;

a word line connected to said memory cell;

a pair of bit lines connected to said memory cell and each having a first capacitance value;

a bit line precharge circuit precharging said pair of bit lines to a power source potential;

a boosted voltage generating circuit generating a voltage of a first potential higher than said power source potential; and

a word line activating circuit receiving said voltage of the first potential from said boosted voltage generating circuit and activating said word line with said voltage of the first potential, wherein

said memory cell includes:

first and second inverters each of which has a load element and a drive element and which are cross-coupled;

a first storage node connected to an output node of said first inverter and an input node of said second inverter and having a second capacitance value which is equal to or larger than 1/8 of said first capacitance value;

a second storage node connected to an output node of said second inverter and an input node of said first inverter and having said second capacitance value; and

first and second gate elements connecting said first and second storage nodes to one bit line in said pair of bit lines and the other bit line, respectively, and

current drivability of said drive element is lower than twice of current drivability of said first and second gate elements.

2. The semiconductor memory device according to claim 1, wherein said memory cell further includes:

a first capacitive element whose one end is connected to said first storage node and whose other end is connected to a constant potential node;

and

a second capacitive element whose one end is connected to said second storage node and whose other end is connected to said constant potential node, and

said first and second storage nodes have said second capacitance value when said first and second capacitive elements are connected to said first and second storage nodes, respectively.

3. The semiconductor memory device according to claim 1, wherein said drive element includes a first transistor of a first conductive type,

said first and second gate elements include second transistors of the first conductive type, and

said load element includes a resistive element formed of polysilicon with high resistance.

4. The semiconductor memory device according to claim 3, wherein said resistive element includes a thin film transistor of a second conductive type.

5. The semiconductor memory device according to claim 3, wherein said second capacitance value is a value such that the potential of said first storage node which is increased by electric charges supplied from said one bit line to said first storage node in the reading operation does not exceed a threshold voltage of said first transistor.

6. The semiconductor memory device according to claim 3, wherein said power source potential is lower than a second potential which is a sum of the value of a threshold voltage of said first transistor and the value of a threshold voltage of said second transistor.

7. The semiconductor memory device according to claim 3, wherein said first potential is higher than a second potential which is higher

than said power source potential by a threshold voltage of said second transistor.

8. The semiconductor memory device according to claim 3, wherein said bit line precharge circuit includes a transistor of the first conductive type receiving the voltage of said first potential by its gate to operate.

9. The semiconductor memory device according to claim 3, wherein said bit line precharge circuit includes a transistor of a second conductive type receiving the voltage of said power source potential by its gate to operate.

10. The semiconductor memory device according to claim 1, further comprising:

an internal power source generating circuit generating an internal voltage of said power source potential with a constant value on the basis of an external power source voltage, wherein

said memory cell and said bit line precharge circuit operate by receiving said internal voltage supplied from said internal power source generating circuit.

11. The semiconductor memory device according to claim 1, wherein said current drivability of said drive element is in a range from 0.8 to 1.2 of said current drivability of said first and second gate elements.

12. A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in a matrix for storing data;

a plurality of word lines arranged in correspondence with rows of said memory cell array;

a plurality of bit line pairs arranged in correspondence with columns of said memory cell array, each bit line having a first capacitance value;

a plurality of bit line precharge circuits each precharging a corresponding pair of bit lines to a power source potential;

a boosted voltage generating circuit generating a voltage of a predetermined potential higher than said power source potential; and

a plurality of word line activating circuits each receiving said voltage of the predetermined potential from said boosted voltage generating circuit and activating a corresponding word line with said voltage of the predetermined potential, wherein

each of said plurality of memory cells includes:

first and second inverters each of which has a load element and a drive element and which are cross-coupled;

a first storage node connected to an output node of said first inverter and an input node of said second inverter and having a second capacitance value which is equal to or larger than 1/8 of said first capacitance value;

a second storage node connected to an output node of said second inverter and an input node of said first inverter and having said second capacitance value; and

first and second gate elements connecting said first and second storage nodes to one bit line in the corresponding pair of bit lines and the other bit line, respectively,

current drivability of said drive element is lower than twice of current drivability of said first and second gate elements, and

when any of said plurality of word lines is activated, the bit line precharge circuit corresponding to the pair of bit lines which perpendicularly cross the activated word line is made inactive.